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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,786	09/26/2003	Richard John Defouw	2003-080-DSK	9670

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,786	DEFOUW ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-39* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-39 are presented for examination in this application (10,672,786) filed on September 26, 2003.

Acknowledgement is made to the Information Disclosure Statement received on September 26, 2003.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-6, 8-9, 15-20, 22-23 and 26-27 are provisionally rejected on the ground of nonstatutory anticipation-type double patenting as being anticipated by claims 1-20 of copending Application No. **10/672,134** as shown and explained in the table below.

10/672,134	10/672,786	EXPLANATION
1 and 5-6	1	Both describe similar features of wear-leveling events on a plurality of blocks by maintaining two modification vectors.
8	2	Both recite the first vector is sorted in descending order and the second vector is sorted in ascending order.
9	3	Both recite the first vector is sorted in ascending order and the second vector is sorted in descending order.
4	4	Both recite pointers to each block descriptor.
4 and 5	5	Both recite maintaining a modification count.
5 and 6	6	Both recite maintaining a total count and a delta count since a previous wear-leveling event.
2	8	Both recite copying data from a block of higher usage to a block of lower usage.
3	9	Both recite copying data from a block of lower usage to a block of higher usage.
14 and 5-6	15	Both describe similar system with features of wear-leveling events on a plurality of blocks by maintaining two modification vectors.
14 and 2	16	Both recite the first vector is sorted in descending order and the second vector is sorted in ascending order.
14 and 3	17	Both recite the first vector is sorted in ascending order and the second vector is sorted in descending order.
14 and 4	18	Both recite pointers to each block descriptor.
14 and 5	19	Both recite maintaining a modification count.
14 and 6	20	Both recite maintaining a total count and a delta count since a previous wear-leveling event.
15	22	Both recite copying data from a block of higher usage to a block of lower usage.
15	23	Both recite copying data from a block of lower usage to a block of higher usage.
14 and 5-6	26	Both describe similar features of wear-leveling events on a plurality of blocks by maintaining two modification vectors.
14 and 5-6	27	Both describe similar features of wear-leveling events on a plurality of blocks by maintaining two modification vectors.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9, 11-13, 15-23 and 25-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bruce et al. (US 6,000,006), and in view of Jou et al. (US 5,568,423).

As to claim 1, Bruce et al. disclose **a method for managing data in a memory device** [Unified Re-Map and Cache-index Table with Dual Write-Counters for Wear-Leveling of Non-Volatile Flash RAM Mass Storage (title)] **having a plurality of blocks** [figure 3 shows a plurality of physical blocks of a memory device], **comprising the steps of**:

maintaining a first vector having block entries sorted in order of number of overall block modifications for each block of the plurality of blocks [figures 7A~7E show that two vectors (TOT_WR'S and INCR_WR'S) are associated with each physical block; a total-write-counter field indicates a total number of write-erase cycles of the block identified by the physical-block-address field (column 3, lines 4-10), and an incremental-write count indicates the number of writes since the last wear-leveling operation that moved the block (abstract); This table includes an erase counter field which is incremented as a page is erased and written. Once a page reaches a threshold erase count, it is moved to an unused page (column 2, lines 20-30); a total-write count indicates a total number of writes to the flash block since manufacture (abstract)];

maintaining a second vector having block entries sorted in order of number of block modifications since a previous wear-leveling event [figures 7A~7E show that two vectors (TOT_WR'S and INCR_WR'S) are associated with each physical block; a

total-write-counter field indicates a total number of write-erase cycles of the block identified by the physical-block-address field (column 3, lines 4-10), and an incremental-write count indicates the number of writes since the last wear-leveling operation that moved the block (abstract); This table includes an erase counter field which is incremented as a page is erased and written. Once a page reaches a threshold erase count, it is moved to an unused page (column 2, lines 20-30); an incremental-write count indicates the number of writes since the last wear-leveling operation that moved the block (abstract)]; **and**

using the first vector and the second vector to determine which of the plurality of blocks should have its associated data relocated to another block [wear-leveling is performed on a block being written when both total and incremental counts exceed system-wide total and incremental thresholds, which are adjusted as the system ages to provide even wear (abstract); figures 7A~7E; the wear-leveling swap thus moves the data for the heavily-used LBA 011 to the lightly-used PBA 101, while the existing data in PBA 101 for LBA 010 is transferred to the cache and then to the heavily-written PBA 111 (column 8, lines 29-39)].

With respect to claim 1, Bruce et al. do not explicitly mention that **the vectors are sorted.**

However, Jou et al. disclose in their invention "Flash Memory Wear leveling System Providing Immediate Direct Access to Microprocessor" a system for equal utilization of blocks of flash memory whereby the usage of each block (the meter field records the count of the erase cycle amounts that have been utilized, column 6, lines

3-5) is sorted so that the system will select the least-used block (based on a count for the next cycle of usage (abstract), and the usage list (i.e., vector) is continuously sorted in order to provide a free list, or priority list, of blocks according to the least amount of usage (column 6, lines 26-35).

Maintaining a sorted list provides an efficient way of identifying the least-used block by avoiding the time-consuming "compare-and-search" process that would be needed otherwise.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefit of keeping a sorted list so that the least-used (or most-used) target can be readily identified, as demonstrated by Jou et al., and to incorporate it into the existing method disclosed by Bruce et al. to further improve the performance of the wear-leveling technique.

As to claims 2-3, Bruce et al. illustrate in figures 7A~7E how the wear-leveling swap moves the data for the heavily-used LBA 011 to the lightly-used PBA 101, while the existing data in PBA 101 for LBA 010 is transferred to the cache and then to the heavily-written PBA 111 (column 8, lines 29-39).

However, the example provided by Bruce et al. is a "compare-and-search" process that is slow and time-consuming and **does not show sorted lists of either ascending or descending order**.

Jou et al. disclose in their invention "Flash Memory Wear leveling System Providing Immediate Direct Access to Microprocessor" a system for equal utilization of blocks of flash memory whereby the usage of each block is sorted so that the system

will select the least-used block for the next cycle of usage (abstract), and the usage list (i.e., vector) is continuously sorted in order to provide a free list, or priority list, of blocks according to the least amount of usage (column 6, lines 26-35).

Further, Jou et al. teach that the list identifications of each block will be arranged according to those starting with the "least used" block down to the "most used" block, which provides a "free block' list which shows the listing of the least used blocks down to the most used blocks (column 4, lines 17-25).

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefit of keeping a sorted list so that the least-used (or most-used) target can be readily identified, as demonstrated by Jou et al., and to incorporate it into the existing method disclosed by Bruce et al. to further improve the performance of the wear-leveling technique.

As to claim 4, Bruce et al. teach that **the block entries for the first and second vectors each comprise a pointer** [figures 7A~7E show that two vectors (TOT_WR'S and INCR_WR'S) are associated with each physical block] **to a block descriptor for each of the plurality of blocks** [figure 5 shows the two counters (TOTAL WR'S, 46 and INCR WR'S, 48) are maintained in a block descriptor (50) for each physical block (44)].

As to claim 5, Bruce et al. teach that **each said block descriptor maintains a modification count for its respective block** [figure 5 shows the two counters (TOTAL WR'S, 46 and INCR WR'S, 48) are maintained in a block descriptor (50) for each physical block (44)].

As to claim 6, Bruce et al. teach that **the modification count comprises a count of total overall modifications (n count) for its respective block and total modifications since a previous wear-leveling event (Delta-n count) for the respective block** [figures 7A~7E show that two vectors (TOT_WR'S and INCR_WR'S) are associated with each physical block; a total-write-counter field indicates a total number of write-erase cycles of the block identified by the physical-block-address field (column 3, lines 4-10), and an incremental-write count indicates the number of writes since the last wear-leveling operation that moved the block (abstract); This table includes an erase counter field which is incremented as a page is erased and written. Once a page reaches a threshold erase count, it is moved to an unused page (column 2, lines 20-30)].

As to claim 7, Bruce et al. teach that **the n count for a first given block in the first vector** [the TOT_WR'S vector shown in figures 7A~7E] **is compared to the n count for a second given block in the second vector to determine which of the first and second blocks is more physically worn** [this comparison process is illustrated in "example of wear-leveling with dual write counters," column 7, lines 64-67; column 8, lines 1-67; column 9, lines 1-37], **and wherein the Delta-n count for the first given block in the first vector** [the INCR_WR'S vector shown in figures 7A~7E] **is compared to the Delta-n count for the second given block in the second vector to determine which of the first and second blocks is more active** [this comparison process is illustrated in "example of wear-leveling with dual write counters," column 7, lines 64-67; column 8, lines 1-67; column 9, lines 1-37], **and further comprising the**

step of swapping contents of the first given block with the second given block if either of the first given block and second given block are both the more physically worn block and the more active block [this process is illustrated in "example of wear-leveling with dual write counters," column 7, lines 64-67; column 8, lines 1-67; column 9, lines 1-37; the wear-leveling swap thus moves the data for the heavily-used LBA 011 to the lightly-used PBA 101, while the existing data in PBA 101 for LBA 010 is transferred to the cache and then to the heavily-written PBA 111 (column 8, lines 29-60); wear-leveling is performed on a block being written when both total and incremental counts exceed system-wide total and incremental thresholds, which are adjusted as the system ages to provide even wear (abstract)].

As to claim 8, Bruce et al. teach **copying data contained in a block having higher usage to a block having lower usage** [the wear-leveling swap thus moves the data for the heavily-used LBA 011 to the lightly-used PBA 101, while the existing data in PBA 101 for LBA 010 is transferred to the cache and then to the heavily-written PBA 111 (column 8, lines 29-39)].

As to claim 9, Bruce et al. teach **copying data contained in a block having lower usage to a block having higher usage** [the wear-leveling swap thus moves the data for the heavily-used LBA 011 to the lightly-used PBA 101, while the existing data in PBA 101 for LBA 010 is transferred to the cache and then to the heavily-written PBA 111 (column 8, lines 29-39)].

As to claim 10, Bruce et al. teach that **the memory device comprises a block header for each of the plurality of blocks, and wherein the second count for each block is maintained in the block header for each respective block** [figures 5-6].

As to claim 11, refer to "As to claim 7."

As to claim 12, refer to "As to claim 7."

As to claim 13, Bruce et al. teach that **the using step comprises the steps of: (i) determining which of a first given block associated with an entry in the first vector and a second given block associated with an entry in the second vector is more physically worn** [the last entry, for LBA=111, has 300,000 total writes (column 8, lines 15-21)];

(ii) **determining which of the first given block and the second given block is more active** [the last entry, for LBA=111, has 300,000 total writes, but only 12,000 incremental writes since PBA 010 was allocated to LBA 111 (column 8, lines 15-21)];

(iii) **if either one of the first given block and the second given block are both the more physically worn block and the more active block** [the last entry, for LBA=111, has 300,000 total writes, but only 12,000 incremental writes since PBA 010 was allocated to LBA 111, perhaps by a wear-leveling swap operation. Although the total writes of 300,000 exceeds the total threshold, the incremental writes of 12,000 is below the incremental threshold of 25,000. Thus PBA 010 is not yet ready for wear-leveling. The sixth entry, for LBA 110, has 200,000 total and incremental writes. It is also not a candidate for wear-leveling, since the total writes has not yet exceeded the total threshold of 250,000. Other pages are also not ready for wear-leveling, having few total

writes (LBA's 001, 010, 101, 110) or not enough incremental writes (LBA's 010, 100, 111). Entry 90, for LBA 011, is ready for wear-leveling, since its total writes has exceeded the total threshold of 250,000, and its incremental writes has also exceeded the incremental threshold of 25,000. The wear-leveling controller searches for a least-used flash block. The physical block with the least total number of writes is PBA 101, with 20,000 total writes. This block is currently allocated to LBA 010. The wear-leveling swap thus moves the data for the heavily-used LBA 011 to the lightly-used PBA 101, while the existing data in PBA 101 for LBA 010 is transferred to the cache and then to the heavily-written PBA 111. (column 8, lines 15-39)], **updating a swap table to indicate that contents of the first given block should be swapped with contents of the second given block** [figure 3 shows the mapping table from a logical block to a physical block; figures 7A~7E show the process of updating a swap table];

(iv) **repeating steps (i) - (iii) for each block entry in at least the first vector** [figures 7A~7E; the repeating procedure is described in detail starting from column 7, lines 64, through column 8 and to column 9, lines 37];

(v) **re-sorting the second vector such that the blocks associated with the block entries contained therein are sorted in order of number of block modifications since a previous wear-leveling event** [illustrated in figures 7A~7E];

(vi) **repeating steps (i) - (iv) for the re-sorted second vector** [figures 7A~7E; the repeating procedure is described in detail starting from column 7, lines 64, through column 8 and to column 9, lines 37]; **and**

(vii) **swapping blocks according to the swap table** [illustrated in figures 7A~7E].

As to claim 15, refer to "As to claim 1."

As to claims 16-17, refer to "As to claims 2-3."

As to claim 18, refer to "As to claim 4."

As to claim 19, refer to "As to claim 5."

As to claim 20, refer to "As to claim 6."

As to claim 21, refer to "As to claim 7" and "As to claim 13."

As to claim 22, refer to "As to claim 8."

As to claim 23, refer to "As to claim 9."

As to claim 25, refer to "As to claim 7" and "As to claim 13."

As to claim 26, refer to "As to claim 1."

As to claim 27, refer to "As to claim 1."

As to claim 28, refer to "As to claim 1." Note that the wear-leveling swap thus moves the data for the heavily-used LBA 011 to the lightly-used PBA 101, while the existing data in PBA 101 for LBA 010 is transferred to the cache and then to the heavily-written PBA 111 (column 8, lines 29-39). In other words LBA 011 and LBA 010 form a block pair. Also refer to "As to claim 7" and "As to claim 13."

As to claim 29, refer to "As to claim 1" and "As to claim 13."

As to claim 30, refer to "As to claim 7" and "As to claim 13."

As to claim 31, refer to "As to claim 7" and "As to claim 13."

As to claim 32, refer to "As to claim 7" and "As to claim 13." Further, figures 7A~7E indicate a total threshold of 250,000 and an incremental threshold of 25,000.

As to claim 33, refer to "As to claim 7" and "As to claim 13." Further, figures 7A~7E indicate a total threshold of 250,000 and an incremental threshold of 25,000.

As to claim 34, refer to "As to claim 6" and "As to claim 7."

As to claim 35, refer to "As to claim 6" and "As to claim 7."

As to claim 36, refer to "As to claim 7" and "As to claim 13."

As to claim 37, refer to "As to claim 1" and "As to claim 13."

As to claim 38, refer to "As to claim 7" and "As to claim 13." Further, figures 7A~7E indicate a total threshold of 250,000 and an incremental threshold of 25,000.

As to claim 39, refer to "As to claim 7" and "As to claim 13." Further, figures 7A~7E indicate a total threshold of 250,000 and an incremental threshold of 25,000.

6. Claims 10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bruce et al. (US 6,000,006), in view of Jou et al. (US 5,568,423), and further in view of Ban (US 6,732,221).

As to claims 10 and 24, Bruce et al. teach using a total count and an incremental count, with both counts indicate erase cycles associated with each block (column 3, lines 4-10).

With respect to claims 10 and 24, Bruce et al. do not mention **using separate counts for indicating erase and write, respectively**.

However, ban discloses in the invention "Wear Leveling of Static Areas in Flash Memory" an improved method for affecting wear leveling in all units of a flash media by launching the wear leveling method once per some large number of write or erase operations done by the flash data manager (abstract), and maintaining one count

indicating the number of write operations (write_count, figures 2 and 4) and another count indicating the number of erase operations (erase_count, figures 3 and 5) for each of the block.

Maintaining two counts, one for write operations and the other for erase operations, provides more information regarding the particular type of usages on the blocks and allow wear leveling events to be performed according to the type of usages, hence improving the flexibility of the wear leveling method.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefit of Maintaining two counts, one for write operations and the other for erase operations, as demonstrated by Ban, and to incorporate it into the existing method disclosed by Bruce et al. to further improve the flexibility of the wear-leveling technique.

Allowable Subject Matter

7. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Chang et al., (US 6,973,531), "Tracking the Most Frequently Erased Blocks in Non-Volatile Memory Systems."

- Chang et al., (US 6,831,865), "Maintaining Erase Counts in Non-Volatile Storage Systems."
- Chen et al., (US 6,944,063), "Non-Volatile Semiconductor Memory with Large Erase Blocks Storing Cycle Counts."
- Lofgren et al., (US 6,230,233), "Wear Leveling Techniques for Flash EEPROM Systems."

Conclusion

9. Claims 1-13 and 15-39 are rejected as explained above.

10. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

December 18, 2005

PIERRE BATAILLE
PRIMARY EXAMINER
3/8/06